## **ACKNOWLEDGEMENT RECEIPT**

## **Electronic Version**

Stylesheet Version v01

Title of Invention

EFS ID:

SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING

Submision Type : Utility Patent Filing

Application Number:

10/604731

45500

Server Response:



Confirmation Code	Message
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First Named Applicant: Geng Wang

Attorney Docket Number: FIS920030209US1

Timestamp: 2003-08-13 13:42:02 EDT

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